Title: **METHOD AND VLSI CIRCUITS ALLOWING TO CHANGE DYNAMICALLY THE LOGICAL BEHAVIOUR**

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Priority: CANADA (Priority CA 2,338,458)

AMENDMENT BEFORE ACTION

This is an Amendment submitted at the time of filing. If additional fee is required, please advice and it will be paid immediately.

In the Description: Please insert at page 15 before the last paragraph, the following text:

"If the combinational circuit is expressed by a single sum-of-product logical equation (r = 1) and implemented according to the invention, a simpler structure of the VLSI circuit **40** can be used, as shown in Figure 11 for the following logical equation:

$$L = \overline{x} \cdot \overline{y} + \overline{y} \cdot \overline{z} + x \cdot y \cdot z. \qquad (8)$$

The simplified basic cell **101** has in this example only the mask word register (**32**) and the product word register (**33**) connected to the associated combinational part, formed by AND gates **35**, EQUIVALENCE (XNOR) gates **36**, and AND gate **37**. One and only one final OR gate **39** is used to determine the output. For simplification, all the registers in Figure 11 are considered with 3 bits capacity, but it is understood that the size of words is selected according to the exemplary equation".

In the Drawings: Please add Figure 11, enclosed.

In the Claims:

3 (Amended) A [cell C(k) as defined in claim **2**] VLSI circuit as in claim **1**, wherein said storage area of a cell C(k) comprises [three] m-bit registers for m input bits of said C(k) cell.

4 (Amended) A [cell C(k) as defined in claim **2**] VLSI circuit as in claim **1**, wherein said first AND gates of a cell C(k) comprises m (2-bit AND gates) for m input bits to produce said first intermediate result [for m input bits].

5 (Amended) A [cell C(k) as defined in claim **2**] VLSI circuit as in claim **1**, wherein said EQUIVALENCE gates of a cell C(k) comprises m (2-bit EQUIVALENCE [(~~XOR~~)] (XNOR) gates) for m input bits to produce said second intermediate result [for m input bits].

6 (Amended) A [cell C(k) as defined in claim **2**] VLSI circuit as in claim **1**, wherein said second AND gate of a cell C(k) comprises one m-bit AND gate for m input bits to produce a logical value which is the value of the product term [for m input bits].

7 (Amended) A [cell C(k) as defined in claim **2**] VLSI circuit as in claim **1**, wherein said third AND gates of a cell C(k) comprises m (2-bit AND gates) for m input bits to allow passing said function word if said product term has the logical value of 1 [for m input bits].

8 (Amended) A VLSI circuit according to claim [**2**] **1** for implementing in hardware any synchronous sequential circuit with clock input only and outputs taken from the state register, having the next state functions expressed in logical sum-of-product equations, with [m] s bits in state register and n product terms p(k), further comprising:

a clock input;

a state register with [m] s bits for storing the state variables;

n cells of said cell C(k) for determining the logical value of a product term p(k) of said next state equations;

a logical summing circuit, realised with [m] s OR gates each one with n inputs, associated with said cell C(k) for receiving the logical value of product terms p(k) and outputting the [m] s bits of said next state functions;

a feedback connection to establish the next state.

9 (Amended) A VLSI circuit according to claim [**2**] **1** for implementing in hardware any synchronous sequential circuit with data inputs and clock input, having the next state functions and the output functions expressed in logical sum-

of-product equations, with m inputs, r outputs, s bits in state register, n1 product terms p(k) in next state equations and n2 product terms p(k) in output equations, further comprising:

a clock input;

a register with m bits for storing the input variables;

a state register with s bits for storing the state variables;

n1 cells of said cell C(k) for determining the logical value of a product term p(k) of said next state equations;

n2 cells of said cell C(k) for determining the logical value of a product term p(k) of said output equations;

a logical summing circuit, realised with [(m + s)] s OR gates each one with n1 inputs, associated with said cell C(k) for receiving the logical value of product terms p(k) of the next state equations and outputting the [(m + s] s bits of next state functions.

a logical summing circuit, realised with r OR gates each one with n2 inputs, associated with said cell C(k) for receiving the logical value of product terms p(k) and outputting the r bits of output functions.

a feedback connection to establish the next state;

11 (Amended) A method for dynamically configuring the logical behaviour of a VLSI circuit as described in claim **1**, [or] and a VLSI circuit as described in claim **8**, [or] and a VLSI circuit as described in claim **9**, by performing the steps of:

inputting the name of input variables, the name of outputs and a plurality of sum-of –product equations, which describe the logical behaviour of a digital circuit, to an expert system as defined in claim **10**;

generating [three] memory words uniquely defining each product term of said equations, as defined in claim **10**; and

storing [said mask word, said product word, and said function word] each memory word into a corresponding register associated with a cell C(k).

12 (New) A VSLI circuit as defined in claim **1**, wherein if said VLSI circuit has one output (r=1), said cell C(k) comprises: